

CLAIMS

We claim:

1 1. A clock generator comprising:
2 a first circuit adapted to programmably receive an input
3 signal, having a possible range of voltage levels and signal
4 types, and modify a frequency of the input signal by a first
5 programmable amount to generate a first input signal;
6 a feedback loop circuit adapted to receive a feedback
7 signal and modify a frequency of the feedback signal by a second
8 programmable amount to generate a second input signal;
9 a phase-locked loop circuit adapted to receive the first
10 input signal and the second input signal and provide a first
11 output signal; and
12 a second circuit adapted to receive the first output signal
13 and modify a frequency of the first output signal to generate a
14 plurality of second output signals having programmable
15 frequencies, wherein the first and second programmable amount
16 and the programmable frequencies are determined by data stored
17 in electrically erasable memory.

1 2. The clock generator of Claim 1, further comprising
2 input/output boundary scan circuits adapted to provide JTAG test
3 support for the clock generator.

1 3. The clock generator of Claim 2, wherein the JTAG test
2 support provides IEEE 1149.1 compliance.

1 4. The clock generator of Claim 1, wherein the clock
2 generator is in-system programmable.

1 5. The clock generator of Claim 4, wherein the clock
2 generator is in-system programmable by supporting IEEE 1532
3 standards.

1 6. The clock generator of Claim 1, wherein the feedback
2 signal is selected from an internal feedback signal and an
3 external feedback signal.

1 7. The clock generator of Claim 1, wherein the phase-
2 locked loop circuit generates a lock signal when the first input
3 signal and the second input signal are frequency and phase
4 locked.

1 8. The clock generator of Claim 1, wherein the first
2 circuit comprises three buffers adapted to programmably accept
3 single and differential signals.

1 9. The clock generator of Claim 1, wherein the signal
2 types comprise single-ended signals and differential signals.

1 10. The clock generator of Claim 1, further comprising a
2 plurality of output circuits adapted to receive the plurality of
3 second output signals and programmably provide a plurality of
4 third output signals having a range of selectable voltage
5 levels, signal types, and output impedance.

1 11. The clock generator of Claim 10, wherein the output
2 circuits are adapted to provide a flexible output banking
3 structure.

1 12. The clock generator of Claim 1, further comprising a
2 plurality of multiplexers that are controlled to select from the
3 electrically erasable memory, which determines the frequency of
4 the first input signal, the second input signal, and the second
5 output signals.

1 13. An integrated circuit comprising:

2 means for selecting from a plurality of input signals and
3 generating a first input signal having a programmable frequency;

4 means for selecting from a plurality of feedback signals
5 and generating a second input signal having a programmable
6 frequency;

7 a phase-locked loop adapted to receive the first input
8 signal and the second input signal and generate a first output
9 signal;

10 means for receiving the first output signal and generating
11 second output signals having programmable frequencies;

12 means for selecting from the second output signals and
13 providing output signals each having a programmable voltage
14 level, signal type, and output impedance; and

15 means for providing configurability and in-system
16 programmability.

1 14. The integrated circuit of Claim 13, further comprising
2 means for testing the integrated circuit to provide IEEE 1149.1
3 compliance.

1 15. The integrated circuit of Claim 13, further comprising
2 means for selecting the programmable frequency for the first
3 input signal and the second input signal and the programmable
4 frequencies for the second output signals.

1 16. The integrated circuit of Claim 13, wherein the signal
2 type comprises single-ended signals and differential signals.

1 17. A method of generating clock signals, the method
2 comprising:

3 receiving an input signal, wherein the input signal may be
4 a single-ended signal type or a differential signal type;

5 modifying a frequency of the input signal by an amount
6 determined from data selected from memory to provide a first
7 input signal;

8 receiving a feedback signal;

9 modifying a frequency of the feedback signal by an amount
10 determined from data selected from memory to provide a second
11 input signal;

12 aligning a frequency and/or a phase of the first input
13 signal and the second input signal to provide a first output
14 signal;

15 modifying a frequency of the first output signal to
16 generate a plurality of second output signals having frequencies
17 determined from data selected from memory; and

18 providing output signals, selected from the second output
19 signals, which have programmable voltage levels, signal types,
20 and output impedances.

1 18. The method of Claim 17, further comprising providing
2 configuration data to the memory.

1 19. The method of Claim 17, further comprising providing
2 in-system programmability to modify configuration data stored in
3 the memory.

1 20. The method of Claim 17, further comprising providing
2 JTAG compliant functional testing.

1 21. A clock generator comprising:

2 an input circuit programmable to receive input signals of

3 various signal types and voltage levels and to generate in

4 response an input signal to a phase-locked loop (PLL);

5 a phase-locked loop adapted to receive the PLL input signal

6 and to generate in response a PLL output signal; and

7 an output circuit adapted to receive the PLL output signal

8 and be programmable to generate in response clock signals of

9 various signal types and voltage levels.

1 22. The clock generator of Claim 21, further including a

2 clock divider circuit coupled between the input circuit and the

3 phase-locked loop and programmable to modify a frequency of the

4 PLL input signal.

1 23. The clock generator of Claim 21, further including a

2 clock divider circuit coupled between the phase-locked loop and

3 the output circuit and programmable to modify a frequency of the

4 PLL output signal.

1 24. The clock generator of Claim 21, further including a

2 feedback loop circuit programmable to modify a frequency of a

3 feedback signal and to provide the modified signal as a second

4 PLL input signal.

1 25. The clock generator of Claim 21, further comprising
2 input/output boundary scan circuits adapted to provide JTAG test
3 support.

1 26. A method of generating a clock signal, the method
2 comprising:

3 programmably receiving input signals of various signal
4 types and voltage levels and generating an input signal for a
5 phase-locked loop (PLL);

6 receiving the PLL input signal and generating in response a
7 PLL output signal; and

8 receiving the PLL output signal and programmably generating
9 in response clock signals of various signal types and voltage
10 levels.

1 27. The method of Claim 26, further comprising
2 programmably modifying a frequency of the PLL input signal.

1 28. The method of Claim 26, further comprising
2 programmably modifying a frequency of the PLL output signal.

1 29. The method of Claim 26, further comprising
2 programmably modifying a frequency of a feedback signal and
3 providing the modified signal as a second PLL input signal.

- 1 30. The method of Claim 26, further comprising providing
- 2 JTAG support and IEEE 1532 in-system programmable standards.